UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,595	12/28/2001	Guy L. Steele JR.	06502.0365	2867

60667 7590 12/27/2006

SUN MICROSYSTEMS/FINNEGAN, HENDERSON LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
MAI, TAN V	
ART UNIT	**PAPER NUMBER**
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
2 MONTHS	12/27/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

MAILED

[illegible] 2006

Technology Center 2100

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/035,595
Filing Date: December 28, 2001
Appellant(s): STEELE, GUY L.

Nathan A. Sloan
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed April 07, 2006 appealing from the Office action mailed May 31, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

The Appeal of U.S. Patent Application No. 10/035,579.

The Appeal of U.S. Patent Application No. 10/035,747.

The Appeal of U.S. Patent Application No. 10/035,584.

The Appeal of U.S. Patent Application No. 10/035,587.

The Appeal of U.S. Patent Application No. 10/035,647.

The Appeal of U.S. Patent Application No. 10/035,580.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

This appeal involves claims 1-5 and 7-40.

Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The modifications are as follows:

Claims 1-5 and 7-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al.

It is noted that upon further review of the claims and the Huang et al. patent, it has been determined that Huang et al. anticipates the invention as recited in claims 1-5 and 7-40 currently under appeal. The grounds of rejection section of this Examiner's Answer sets forth the modified rejection of claims 1-5 and 7-40 in view of Huang et al.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,995,991	HUANG ET AL.	11-1999
6,009,511	LYNCH ET AL.	12-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

(10) Following is a reproduction of Final Rejection of claims 1-5 and 7-40 in view of the Lynch reference and the modified rejection in view of the Huang et al. reference :

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

B. Claims 1-5 and 7-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al.

As per independent claim 1, Huang et al disclose, e.g., see **Fig. 4**, the invention, **arithmetic calculation circuit (100)**, substantially as claimed, including: **X and Y operand registers 116 & 118; arithmetic section 114 and special operand generator 122**. Huang et al's disclosed X and Y operand registers each includes a special operand indicator (116-2 and 118-2) which is stored as special operand of a

predetermined set of special operands. It is noted that although Huang et al do not refer to an "analyzer circuit" per se, Huang et al.'s device is configured to determine a **first status** of a first floating point operand and a **second status** of a second floating point operand, similar to the function of the claimed analyzer circuit, thus Huang et al.'s arithmetic **calculation circuit (100)** having special operand indicator in each operand register corresponds to the "analyzer circuit" as claimed.

As per dependent claim 2, the claim adds: (1) "first / second operand buffer" and (2) "first / second operand analysis circuit". The memory (register file) 112 in Huang's Fig. 4 corresponds to the claimed "operand buffer", since a buffer is nothing more than a storage for temporary storing desired data, and Huang's disclosed register file 112 clearly store operands at least temporarily. Second, Huang et al's **arithmetic calculation circuit (100)** , specifically arithmetic section 114 inherently includes circuit(s) for determining the first / second status as claimed.

As per dependent claim 3, the claim adds the "first status and the second status are determined without regard to memory storage external to the first operand buffer and the second operand buffer". Huang et al disclose a similar feature, i.e., "X and Y operand registers each includes a special operand indicator which is stored a special operand of a predetermine set of special operands feature".

As per dependent claim 4, the claim adds the "memory storage external ...is a floating point status register". Huang et al. disclose special floating point operands, thus the register file 112 includes floating point registers (for storing status information e.g. of output of 150), as claimed.

As per dependent claim 5, the claim details the "results circuit". Huang et al's arithmetic section 114 , tag generator 150 and special operand generator 122 in combination provide the "resulting floating point operand and embed the resulting status" as claimed, since they produce the resulting floating point operand along with the resulting tag to be stored within the register file 112 (thus embedding the status, i.e. tag within the resulting operand stored in the register file 112).

As per dependent claim 7, the claim adds "the sum ... is identical in all cases to the sum would be produced if the two operands were first swapped". The feature is inherent in the addition of operands in Huang (e.g. "add" in col. 7 line 52), since addition is a commutative operation, i.e. the sum is identical when the operands are swapped.

As per claim 8,. Huang et al disclose the claimed list of status e.g. in col. 7 lines 20-22

As per dependent claim 9-14, the claim adds the details of the status. These features are disclosed in col.1 lines 55-60 & col. 7 lines 20-23 , table 1 in col. 6, col.1 lines 55-60 & col. 7 lines 20-23, table 1 in col. 6, col. 6 lines 39-43 and col. 9 lines 25-30 respectively.

Due to the similarity of claims 15-40 to claims 1-5 and 7-14, they are rejected under a similar rationale.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

C. Claims 1-5 and 7-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch et al.

As per independent claim 1, Lynch et al disclose, e.g., see **Fig. 4**, the invention, **floating point unit (36)**, substantially as claimed, including: **Register Stack (84) and FPU Core (94)**. Although Lynch et al do not explicitly describe an "analyzer circuit" per se, Lynch's disclosed floating point system is configured to determine a **first status** of a first floating point operand and a **second status** of a second floating point operand ("whether each floating point operand is a normal floating point number or a special floating point number" in abstract, lines 1-7), as recited in the instant claim, thus Lynch's floating point unit in Lynch's system inherently includes an analyzer circuit for performing the determination. Lynch et al. do not explicitly disclose that the resulting status tag is embedded within the resulting floating point operand, as claimed. Lynch et al. do disclose in Fig. 6 that the register stack (84) for storing operand includes result operand having a tag field (89) within the operand for storing appended tag values (see the bridging paragraph of cols. 15 and 16). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to store the floating

point result with its tag as a resulting operand in Lynch's register stack (84) in order to quickly determine its status in subsequent operations.

As per dependent claim 2, the claim adds: (1) "first / second operand buffer" and (2) "first / second operand analysis circuit". First, the "operand buffer" feature is well known in the art for temporary storing desired data. Therefore, including buffers in Lynch's floating point system would have been obvious to one of ordinary skill in the art in order to avoid error due to logic switching of operands. Second, Lynch et al's floating point unit (36), should have circuit(s) for determining the first / second status as claimed.

As per dependent claim 3, the claim adds the "first status and the second status are determined without regard to memory storage external to the first operand buffer and the second operand buffer". In Lynch's floating point system modified in the manner set forth above would includes determining the status of the operand in the floating point core (see abstract), thus without regard to the external memory st=orage as claimed.

As per dependent claim 4, the claim adds the "memory storage external ...is a floating point status register". The feature is inherent in Lynch's floating point unit for indicating the special floating point operands.

As per dependent claim 5, the claim details the "results circuit". Lynch et al's floating point unit (36) modified in the manner set forth above, is capable of providing the "resulting floating point operand and embed the resulting status" as claimed, therefore, inherently includes a "circuit" for performing the operations.

As per dependent claim 7, the claim adds "the sum ... is identical in all cases to the sum would be produced if the two operands were first swapped". Theis feature is inherent in the ADD operation (col. 21, line 18) performed by the floating point unit in Lynch, since addition is a commutative operation, i.e. the sum is identical when the operands are swapped.

As per claim 8, the claim adds the list of status. Lynch et al disclose the equivalent feature, e.g., col. 2, second complete paragraph.

As per dependent claims 9-14, the claim adds the details of the status. Lynch discloses these features in Fig. 5.

Due to the similarity of claims 15-40 to claims 1-5 and 7-14, they are rejected under a similar rationale.

(11) Response to Argument

Appellant's arguments filed April 07, 2006 have been fully considered but they are not persuasive. Appellant argues that:

B1. Claims 1-5 and 7-40 patentably distinguish from Huang

"Huang does not disclose each and every element of Appellant's claimed invention. Independent claim 1 calls for a combination including, for example, 'an

analyzer circuit configured to determine a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively,' (emphasis added)...

First, the Examiner has not identified specific teachings in Huang which show the Examiner's coined term 'special operand indicator.' The Examiner has also not made clear how such alleged teachings relate to, for example, the claimed 'determine a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively" as recited by claim 1 (emphasis added).

Second, even assuming the Examiner's coined term 'special operand indicator' refers to a tag value of Huang (Huang, FIG. 4, 116-2), Huang's teaching of a 'tag value' does not constitute a teaching or suggestion of 'data within the first floating point operand and data within the second floating point operand' (emphasis added) as recited by claim 1...

Moreover, independent claim 1 recites a combination also including, for example, 'a results circuit coupled to the analyzer circuit and configured to ... a resulting status embedded within the resulting floating point operand' (emphasis added). Huang does not teach or suggest at least this additional element.

First, the Examiner has not identified any specific teachings of Huang which would allegedly teach or suggest 'a resulting status embedded within the resulting ... operand,' as recited by claim 1 (emphasis added). See Office Action mailed September

22, 2004 at pp. 3-4. For at least this reason, the Examiner's rejection is improper.

Second, Huang does not teach or suggest 'a resulting status embedded within the resulting floating point operand,' as recited by claim 1 (emphasis added). Rather, as illustrated in FIG. 4, Huang teaches a tag generator 150 to generate the tag (alleged status) separately from the operand, which is loaded separately into tag value portion 116-2 as discussed above. Such teachings by Huang do not constitute a teaching or suggestion of 'a resulting status embedded within the resulting floating point operand,' as recited by claim 1 (emphasis added)."

B2. Claims 9-14, 22-27 and 35-40 patentably distinguish from Huang

"Huang does not disclose each and every element of dependent claims 9-14. In fact, the Examiner has not addressed any of the elements recited by dependent claims 9-14, other than to say that '[t]hese features are obvious design choice.' See Office Action mailed September 22, 2004 at p. 5. This bare assertion fails to meet the requirement for showing how Huang allegedly teaches or suggests each and every element of claims 9-14. Moreover, the Examiner has not identified any motivation in the cited references to make the alleged design choice modification. Id."

C1. Claims 1-5 and 7-40 patentably distinguish from Lynch

"[f]irst, the Examiner has not explained how Lynch's 'tag values' relate to, for example, determining a "first status ... based upon data within the ... operand,' as recited by claim 1. Even if Lynch's tag value were to constitute the claimed 'status,'

(which Appellant does not concede) the tag value of Lynch is not 'data within the ... operand,' as recited by claim 1.

Fig. 4 of Lynch, which Appellant reproduces below, clearly illustrates that Tag Field 89 (alleged status) and Reg Field 87 (operand) are separate from each other and are stored within register stack 84.

Moreover, Lynch specifically states that element 84 is a register stack, not an operand. Lynch, col. 14, lines 47-48. Lynch also states that register stack 84 contains a Reg Field 87 for storing an operand separate from a Tag Field 89 for storing a tag (alleged status). See Lynch, col. 15, lines 63-67. 'Separate from' cannot constitute 'data within' the operand, as recited by claim 1.

Moreover, independent claim 1 recites a combination including, for example, 'a results circuit coupled to the analyzer circuit and configured to ... a resulting status embedded within the resulting floating point operand' (emphasis added). Lynch does not teach or suggest at least this additional element.

First, the Examiner has not addressed this element or identified any specific teachings of Lynch which would allegedly teach or suggest 'a resulting status embedded within the resulting ... operand,' as recited by independent claim 1. See Office Action mailed September 22, 2004 at pp. 5-6. For at least this reason, the Examiner's rejection is improper.

Second, Lynch does not teach or suggest 'a resulting status embedded within the resulting ... operand,' as recited by independent claim 1 (emphasis added). Rather, as discussed above, Lynch teaches that the tag value (alleged status) in Tag Field 89 is

separate from an operand Reg Field 87. Lynch teaches that '[a] tag value is appended to each floating point number stored in a floating point register' (Lynch, col. 5, lines 44-45 (emphasis added)). Such teachings by Lynch do not constitute a teaching or suggestion of 'a resulting status embedded within the resulting ... operand,' as recited by claim 1 (emphasis added)."

C2. Claims 9-14, 22-27 and 35-40 patentably distinguish from Lynch

"Lynch does not disclose each and every element of dependent claims 9-14. As with Huang, discussed above, the Examiner has not addressed any of the elements recited by dependent claims 9-14, other than to say that '[t]hese features are obvious design choice.' See Office Action mailed September 22, 2004 at p. 7. This bare assertion fails to meet the requirement for showing how Lynch allegedly teaches or suggests each and every element of claims 9-14. Moreover, the Examiner has not provided any motivation to make the alleged design choice modification. Id."

With respect to the arguments, the examiner carefully reviews Appellant's specification, drawings, claimed invention and the applied references.

B1. Claims 1-5 and 7-40

It is noted that "X" SPECIAL OPERAND INDICATOR (x_tag) and "Y" SPECIAL OPERAND INDICATOR (y_tag) of Fig. 4 are equivalent to the claimed "determine a **first status** ... and **second status**" feature (e.g., see Abstract, lines 7-10; and claim 1, para. (a) for detail of the tag). According to Fig. 4, "X" (116-1) and "x_tag" (116-2) are belonged to a "X" register (116). In col. 6, lines 64-65, Huang specifically states "**X** and Y **operand** registers 116 and 118 ...". Therefore, it is clearl that Huang's teaching of a "tag value" does constitute a teaching data within the floating point **operand** as claimed. Although the tag generator (150) to generate the tag value separately from the output of arithmetic section (114), the examiner believes that the resulting status "tag value" embedded within the "resulting floating point operand". It is noted that the format [resulting status embedded within the resulting floating point operand] of **stored data** in the MEMORY (REGISTER FILE) 112 is the **same as** the format [status data within the floating point operand] of **data transferred** to "X" or "Y" register because the **read out / write in data** is usually unchanged. Therefore, the **stored** "resulting floating point operand" includes the "resulting status" as claimed.

B2. Claims 9-14, 22-27 and 35-40

As pointed out in the rejection of above claims in this Examiner's answer, Huang discloses "status" information, e.g., zero, overflow, underflow, etc. status flags (e.g. col. 7, lines 20-23); Not a number, etc. (TABLE 1). Also, Huang' s claim 3 discloses "positive infinity" & "negative infinity" features as Appellant's claim 14.

C1. Claims 1-5 and 7-40

It is noted that the "Tag Field" (89) contains the "status" information of each register of Register Stack (84), e.g., see Abstract. According to Fig. 4, "Reg Field" (87) and "Tag Field" (89) are belonged to Register Stack (84). Therefore, it is clearl that Lynch's teaching of a "tag value" does constitute a teaching data within the floating point **operand** as claimed. Although the tag value is appended to each floating point number before being stored in a floating point register stack as set forth in the rejection of claims in this Examiner's Answer, the examiner interprets the floating point register within the register stack as an operand, when appended with the tag value and stored in the register stack. Therefore, that the resulting status "tag value" is embedded within the "resulting floating point operand", when the operand along with the tag value is stored in the register stack in the manner set forth in the rejection.

C2. Claims 9-14, 22-27 and 35-40

As pointed out in the rejection of claims in this Examiner's Answer, Lynch teaches the claimed "status" information, e.g.;"[t]ypes of special floating point numbers include zero, +infinity, -infinity and NaNs" (col. 17, lines 6-7) and Fig. 5. In col. 18, first complete paragraph, Lynch discloses "+infinity" & "-infinity" features as Appellant's claim 14.

(12) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(13) For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Tan V. Mai

Primary Examiner

Conferees:

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 21[illegible]

Kakali Chaki (SPE. Art Unit 2193)

TUAN DAM
SUPERVISORY PATENT EXAMINER

Tuan Dam (SPE. Art Unit 2192)